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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,503	10/31/2003	William Andrew Nevin	7335	3579

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Attn: Matthew E. Comnors
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EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,503	NEVIN ET AL.	
	Examiner	Art Unit	
	Hsien-ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-42 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-14,18-22,26-38,41 and 42 is/are rejected.

7)☒ Claim(s) 15-17,23-25,39 and 40 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

HSIEN-MING LEE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6, 9, 21-22, 29-31, 35, 37, 41 and 42 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al. (US 2004/0198038).

In re claims 1, 29, 37, Huang et al. teach the claimed method for forming a filled trench in a semiconductor layer of a semiconductor substrate, with the effect of trench voids minimized, the method comprising the steps of:

- forming a trench 105 in the semiconductor layer 100 (*silicon*, paragraph [0030]) through a first face (i.e. the top surface of the semiconductor layer 100) thereof, the trench defining an open mouth (Fig.4B);
- relieving the trench 105 adjacent the open mouth thereof for preventing the commencement of bridging of the trench 100 (i.e. relieving the trench 105 by rounding the upper corner of the trench 105 to form a tapered edge 110 and thus to form a relieved trench 105a, Fig.4E) with a filling material 118 (Fig.4H) at a level adjacent the first face of the semiconductor layer 100 as the relieved trench 105a being filled; and

- filling the relieved trench 105a through the open mouth with the filling material 118 (Fig.4H), wherein the filling material is *silicon oxide* (paragraph [0039]).

In re claim 2, Huang et al. teach that the relieved trench 105a is sufficiently relieved for preventing commencement of bridging of the trench 105 with the filling material 118 at a level above a plane extending parallel to and below a plane to which the first face of the semiconductor layer to be finished (Fig.4H), i.e. the trench 105 is sufficiently relieved by forming the tapered corner 110 to form the relieved trench 105a for preventing commencement of bridging of the trench 105 with the filling material 118 being filled above and below the plane parallel to the top surface of the semiconductor layer 100.

In re claim 3, Huang et al. teach that the trench 105 is relieved to form the relieved trench 105a adjacent the open mouth thereof on one side (i.e. left side) of the trench 105 (Fig.4E).

In re claim 4, Huang et al. teach that the trench 105 is relieved to form the relieved trench 105a adjacent the open mouth thereof on respective opposite side (i.e. right side) of the trench 105 (Fig.4E).

In re claims 5, 31 and 35, Huang et al. teach that the trench 105a is lined with at least one lining layer 116 formed therein with a lining material (i.e. a thermally *grown oxide*, paragraph [0038]) prior to filling the trench 105a (Fig.4G).

In re claim 6, Huang et al. teach that the trench 105 is relieved by relieving at least one of the lining layers adjacent the open mouth of the trench 105a (Fig.4G), i.e. trench 105 is relieved by forming the relieved trench 105a and by relieving the lining layer 116 via forming the lining layer 116 on the relieved trench 105a adjacent the open mouth of the trench 105.

In re claim 9, Huang et al. teach that the trench 105 is relieved by forming the relieved trench 105a prior to lining the relieved trench 105a with the lining layer 116 (Figs.4F-4G).

In re claims 21 and 22, Huang et al teach that the trench 105 is relieved by RIE etching (paragraph [0036]).

In re claim 30, Huang et al. teach that the filling material 118 is deposited by chemical vapor deposition (paragraph [0039]).

In re claim 41, Huang et al. teach a semiconductor substrate comprising a semiconductor layer 100 having a first face (i.e. top surface) and a filled trench 105a/118 extending into the semiconductor layer 100 through the first face thereof, the relieved trench 105a defining an open mouth and having been relieved adjacent the open mouth prior to filling of the relieved trench 105a with a filling material 118 for preventing the commencement of bridging of the trench with filling material 118 at a level adjacent the first face of the semiconductor layer as the relieved trench 105a being filled therewith (Figs. 4B-4H).

In re claim 42, Huang et al. also teach the claimed semiconductor substrate, comprising:

- a semiconductor layer 100 having a first face (top surface);
- a filled trench 105a extending into the semiconductor layer 100 through the first face thereof, the trench 105a defining an open mouth and having been relieved adjacent the open mouth prior to filling of the trench 105a with a filling material 118 for preventing the commencement of bridging of the trench 105a with filling material 118 at a level adjacent the first face of the semiconductor layer 110 as the trench 105a being filled therewith.

3. Claims 1, 18 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Murakami et al. (US 6,081,662).

In re claim 1, Murakami et al. teach the claimed method for forming a filled trench in a semiconductor layer of a semiconductor substrate, with the effect of trench voids minimized, the method comprising the steps of:

- forming a trench 18 in the semiconductor layer 1 (*silicon,* col.15, line 28) through a first face (i.e. the top surface of the semiconductor layer 1) thereof, the trench defining an open mouth (Fig.26B);
- relieving the trench 18 adjacent the open mouth thereof for preventing the commencement of bridging of the trench 18 (i.e. relieving the trench 18 by first forming the recessed corner 17 of the trench 18 to form a tapered edge 17 and thus to form a relieved trench 17/18, Fig.26B) with a filling material 8 at a level adjacent the first face of the semiconductor layer 1 as the relieved trench 17/18 being filled; and
- filling the relieved trench 17/18 through the open mouth with the filling material 8 (Fig.27A), wherein the filling material 8 is *silicon oxide* or *silicon nitride* (col. 14, lines 2-4).

In re claim 18, Murakami et al. teach that the each side of the trench 18 which is relieved is relieved by forming a relieving recess 17 into the first surface of the semiconductor layer 1 adjacent to and communicating with the trench 18 adjacent to the open mouth (Fig.26B).

In re claim 19, Murakami et al. teach that the relieving recess 17 is concave when viewed in a direction into the trench 18 (Fig.26B).

4. Claims 1, 5, 10, 11, 26, 29, 32 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Wieczorek et al. (US 6,812,115).

In re claims 1 and 29, Wieczorek et al. teach the claimed method for forming a filled trench in a semiconductor layer of a semiconductor substrate, with the effect of trench voids minimized, the method comprising the steps of:

- forming a trench 304 in the semiconductor layer 301/302/303 through a first face (i.e. the top surface of the semiconductor layer 301/302/303) thereof, the trench 304 defining an open mouth (Fig.3b);
- relieving the trench 304 adjacent the open mouth thereof for preventing the commencement of bridging of the trench 304 (i.e. relieving the trench 304 by forming a tapered sidewall portion, Fig.3b) with a filling material 306 (Fig.3f) at a level adjacent the first face of the semiconductor layer 301/302/303 (Fig.3g) as the relieved trench 304 being filled; and
- filling the trench 304 through the open mouth with the filling material 306 (Fig.3g, wherein the filling material 306 is *silicon oxide* (col.8, lines 18-19 and col.1, lines 20-21).

In re claim 5, Wieczorek et al. teach that the trench 304 is lined with at least one lining layer 320 formed therein with a lining material (silicon oxide) prior to filling the trench 304 (Fig.3d).

In re claim 10, Wieczorek et al. teach that the trench 304 is relieved to a depth from the open mouth in the range of 400~500 nm or 0.4~0.5 μm (col. 7, lines 46-48 and col. 2, lines 11-12).

In re claim 11, Wieczorek et al. teach that each side of the trench 304 which is relieved is relieved by tapering a portion of the side of the trench adjacent the open mouth (Fig.3b), each

tapered portion defining a tapering plane which converges towards the other side in a direction into the trench.

In re claim 26, Wieczorek et al. teach that first face (the top surface) of the semiconductor layer 301/302/303 adjacent the trench 304 is lined with the lining material 320 during lining of the trench 304 with at least one of the lining layers 320/330 (Fig.3d).

In re claim 32, Wieczorek et al. teach that at least one 320 of the lining layers 320/330 is a deposited layer (col. 7, lines 54-55).

In re claim 35, Wieczorek et al. teach that at least one 330 of the lining layers 320/330 is a thermally grown layer (col. 7, lines 50-52).

5. Claims 1, 5, 7, 8, 12-14, 20, 26-29, 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Joo (US 6,544,861).

In re claims 1 and 29, Joo teaches the claimed method for forming a filled trench in a semiconductor layer of a semiconductor substrate, with the effect of trench voids minimized, the method comprising the steps of:

- forming a trench 180 in the semiconductor layer 100/160 through a first face (i.e. the top surface of the semiconductor layer 100/160 thereof, the trench 180 defining an open mouth (Fig.4);
- relieving the trench 180 adjacent the open mouth thereof for preventing the commencement of bridging of the trench 180 (i.e. relieving the trench 180 by first forming a lining layer 220 in the trench (Fig.5) and then etching a portion of the lining layer 220 to form a tapered sidewall on the entire trench depth, as shown in

Fig.6) with a filling material 280 (Fig.9) at a level adjacent the first face of the semiconductor layer 100/160 as the relieved trench being filled; and

- filling the trench 180 through the open mouth with the filling material 280 (Fig.9), wherein the filling material 280 is an *oxide* (col., 5, last line through col. 6, line 1).

In re claim 5, Joo teaches that the trench 180 is lined with at least one lining layer 260 formed therein with a lining material prior to filling the trench (Fig.8).

In re claim 7, Joo teaches that the trench 180 is relieved at least the lining layer 220 first formed in the trench 180 (Fig.5) prior to relieving the trench by forming the tapered sidewall portion 240a (Fig.6).

In re claim 8, Joo teaches that the trench 180 is relieved by relieving at least one of the lining layers 200/220 formed after the first 200 of the lining layers 200/220 to be formed (Fig.5).

In re claims 12-14, Joo teaches that the tapering plane defined by each tapered portion 240a/240b defines with a central plane bisecting the trench and extending longitudinally along the trench thorough the open mouth a relief angle in the range of at least larger than 0.2° (claim 12) or 4 ° (claim 13) or 6° (claim 14), as shown in Fig. 6.

In re claim 20, Joo teaches that each side of the trench which is relieved is relieved along the entire length of the trench, i.e. relieving the trench 180 by forming the tapering portions 240a/240b on the sidewall of the trench 180 (Fig.6), wherein the tapering portions 240a/240b are formed along the entire length of the trench 180 (Fig.6).

In re claim 26, Joo teaches that first face (the top surface) of the semiconductor layer 100/160 adjacent the trench 180 is lined with the lining material 260 (Fig.8) during lining of the trench with at least one 260 of the lining layers 200a/240a/260 (Fig.8).

In re claim 27, Joo teaches that the filling material 280 and the lining material 260 above the first face of the semiconductor layer 100/160 are thinned to a level just above the first face (i.e. the top surface) of the semiconductor layer 100/160 (Fig.10).

In re claim 28, Joo teaches that the filling material 280 and the lining material 260 above the first face of the semiconductor layer 100/160 are removed to a level coplanar with the first face (i.e. the top surface) of the semiconductor layer 100/160 (Fig.10).

In re claim 35, Joo teaches that at least one 200 of the lining layers 200/220 is a thermally grown layer (col.4, line 55).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joo (US '861) in view of Dong et al. (US 2004/0102005).

In re claim 36, Joo does not teach that at least one of the lining layers is densified prior to filling of the trench with the filling material.

Dong et al., in an analogous art, teach densifying the deposited lining layer 20 (paragraph 0021]) prior to filling of the trench 18 with the filling material 22.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to densify the deposited lining layer 240a of Joo, as taught by Dong et al.,

prior to filling the filling material 280 in the relieved trench, since by this manner it would provide a better tapered profile in the trench.

8. Claims 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wieczorek et al. (US '115) in view of Chu (US 6,180,493).

In re claim 33, Wieczorek et al. teach that the trench 304 is lined with the lining layer 320 (silicon oxide) prior to filling the trench 304 (Fig.3d) but do not teach that the lining layer is deposited by a TEOS deposition process.

Chu, in an analogous art, teaches forming a TEOS silicon oxide as the lining layer 212 (Fig.2C and col. 4, lines 40-45) in the trench 208 prior to filling the trench 208 with a filling material 216.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to utilize the TEOS process, as taught by Chu, for forming the lining layer of Wieczorek et al., since by this manner it would form the lining layer with good adhesion between the trench and the filling material.

In re claim 34, Wieczorek et al. in view of teach that the lining layer is deposited by a high conformality deposition process because the TEOS-silicon- oxide-lining layer 212 of Chu is conformally deposited over the underlying structure (Fig.2C) and the silicon-oxide lining layer 320 of Wieczorek et al. is a conformal layer (col. 7, lines 60-62).

9. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US '038) in view of Balasubramanian et al. (US 6,468,853).

Huang et al. teach that the semiconductor layer 100 is a silicon but do not disclose it is a single crystal silicon.

Balasubramanian et al., in an analogous art, teach using single crystal silicon as the semiconductor layer 10 (col. 2, lines 47-48) followed by forming a trench 18 in the semiconductor layer 10; forming a lining layer 20 in the trench 18 and filling the trench 18 with a filling material 28.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to use the single crystal silicon, as taught by Balasubramanian et al., as the semiconductor layer of Huang et al., since by this manner it would form a satisfactory trench isolation structure.

Allowable Subject Matter

10. Claims 15-17, 23-25, 39-40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record, either alone or combination, at least neither teaches nor suggests that each tapered portion defines at least *two tapering planes defining respective different relief angles* with the central plane (claim 15); the parameters of the RIE etch are controlled for *minimizing the depth of scallops* formed by the RIE etch (claim 23); the parameters of the etching process are ramped during the etching process for relieving the trench (claim 24); and the semiconductor substrate is a semiconductor layer of a *semiconductor on insulator* structure (claim 39).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (8:00 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-ming Lee
Primary Examiner
Art Unit 2823

March 3, 2005

HSIEN-MING LEE
PRIMARY EXAMINER